Current Status of Phase Change Memory and its Future

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Agenda

- Introduction
- Basic Cell Operation
- Reliability Considerations
- Cell improvement
- Scaling
- Array Operation
- Summary

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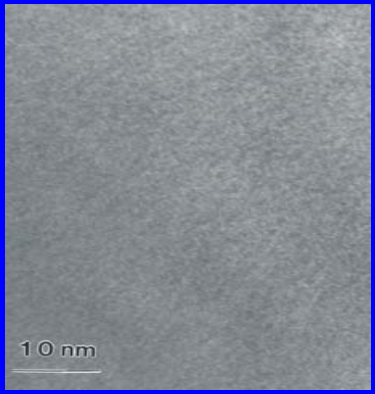
Chalcogenide Material

- Chalcogenide is the general class of switching media in CD-RW and DVD-RW
  - In high volume production and low cost
- Laser beam energy is used to control the switching between crystalline and amorphous phases
  - Higher energy -> amorphous
  - Medium energy -> crystalline
- Low energy laser beam to read

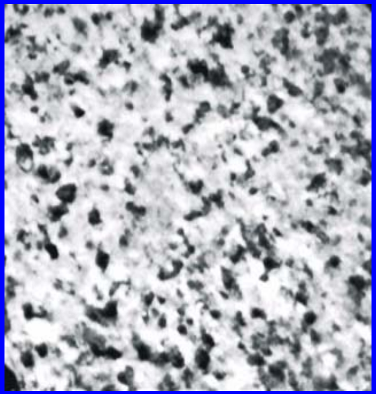
Amorphous vs Crystalline Phases

Amorphous Phase



Scale:

0.2 microns



Crystalline Phase

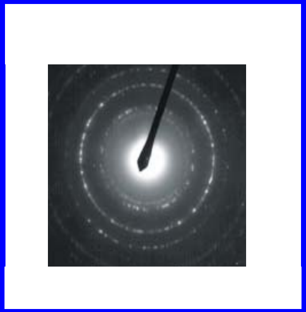
Electron Diffraction Patterns

Short Range Atomic Order

Low Free Electron Density

High Activation Energy

High Resistivity



Long Range Atomic Order

High Free Electron Density

Low Activation Energy

Low Resistivity

Material Characteristics

Phased Change Memory

- Instead of using laser beam, electric current is used to heat the material to switch between amorphous and crystalline phases
  - High current, high temperature: amorphous phase, high resistance
  - Medium current, lower temperature: crystalline phase, low resistance
- Low current to sense resistance

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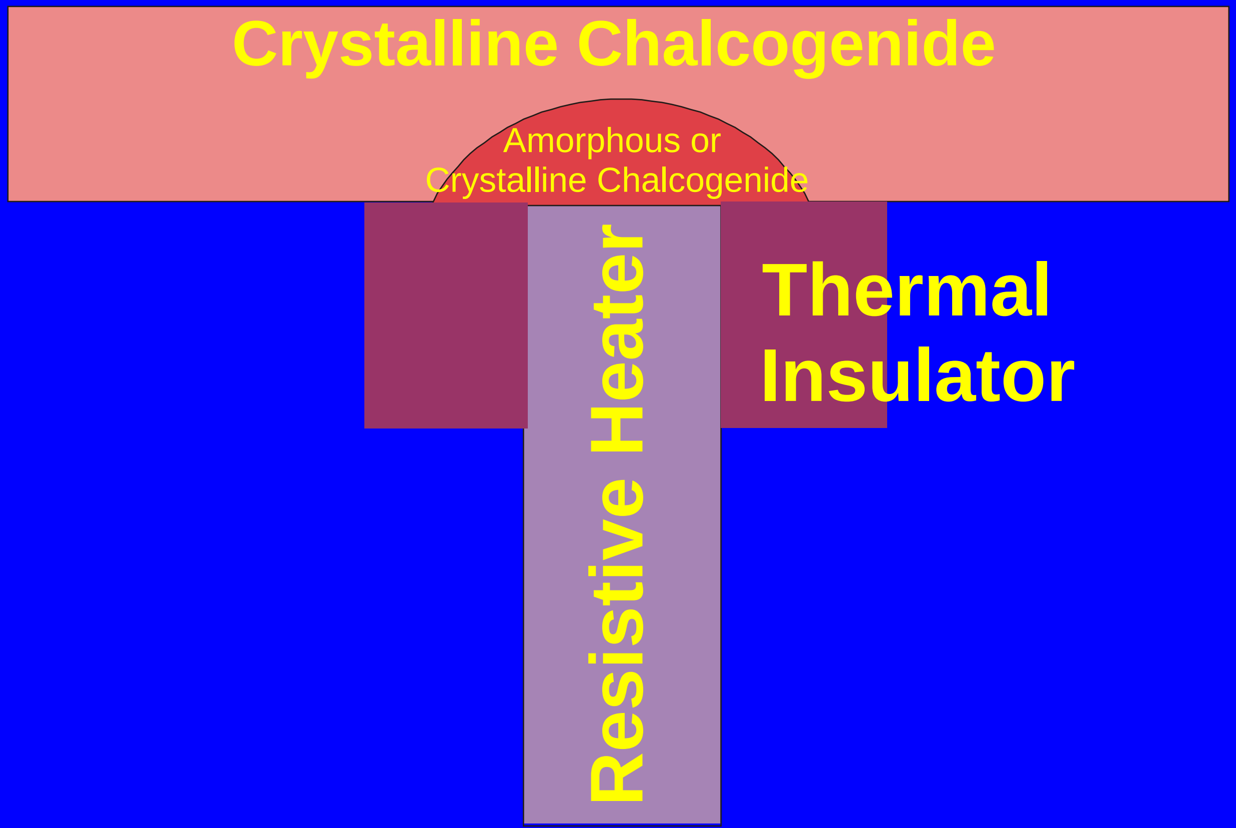
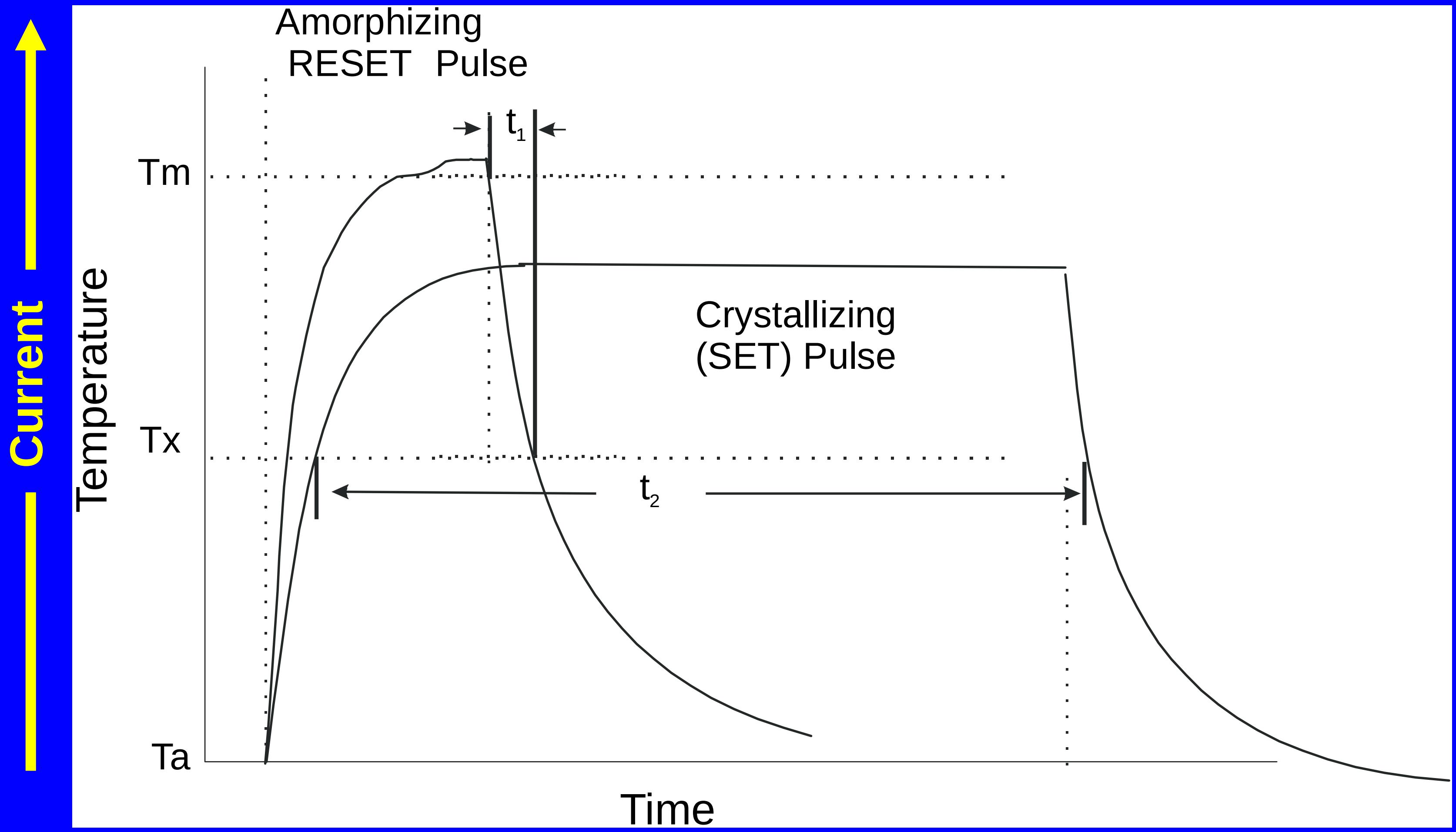
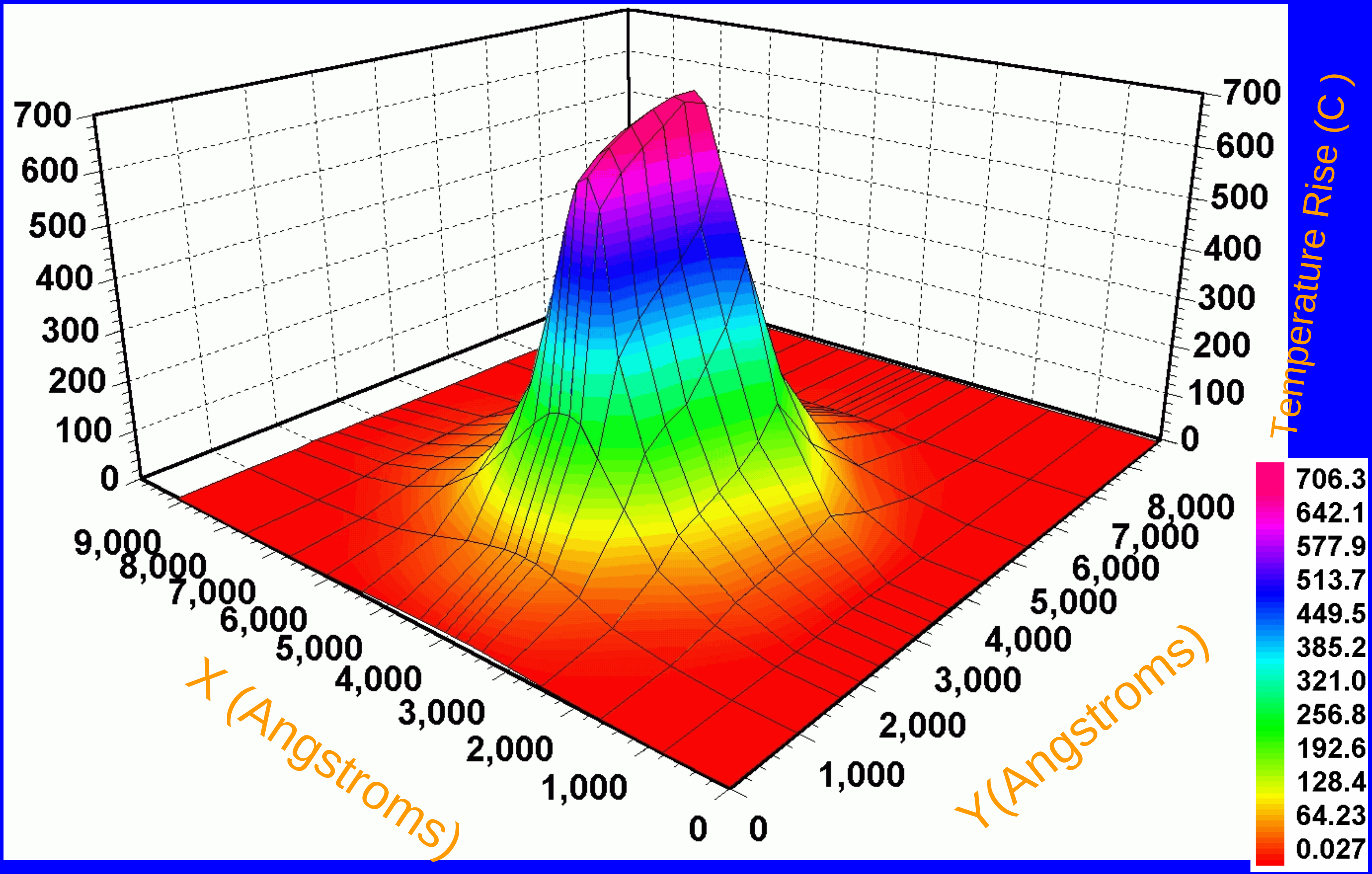
Current Memory Structure



Basic Device Operation

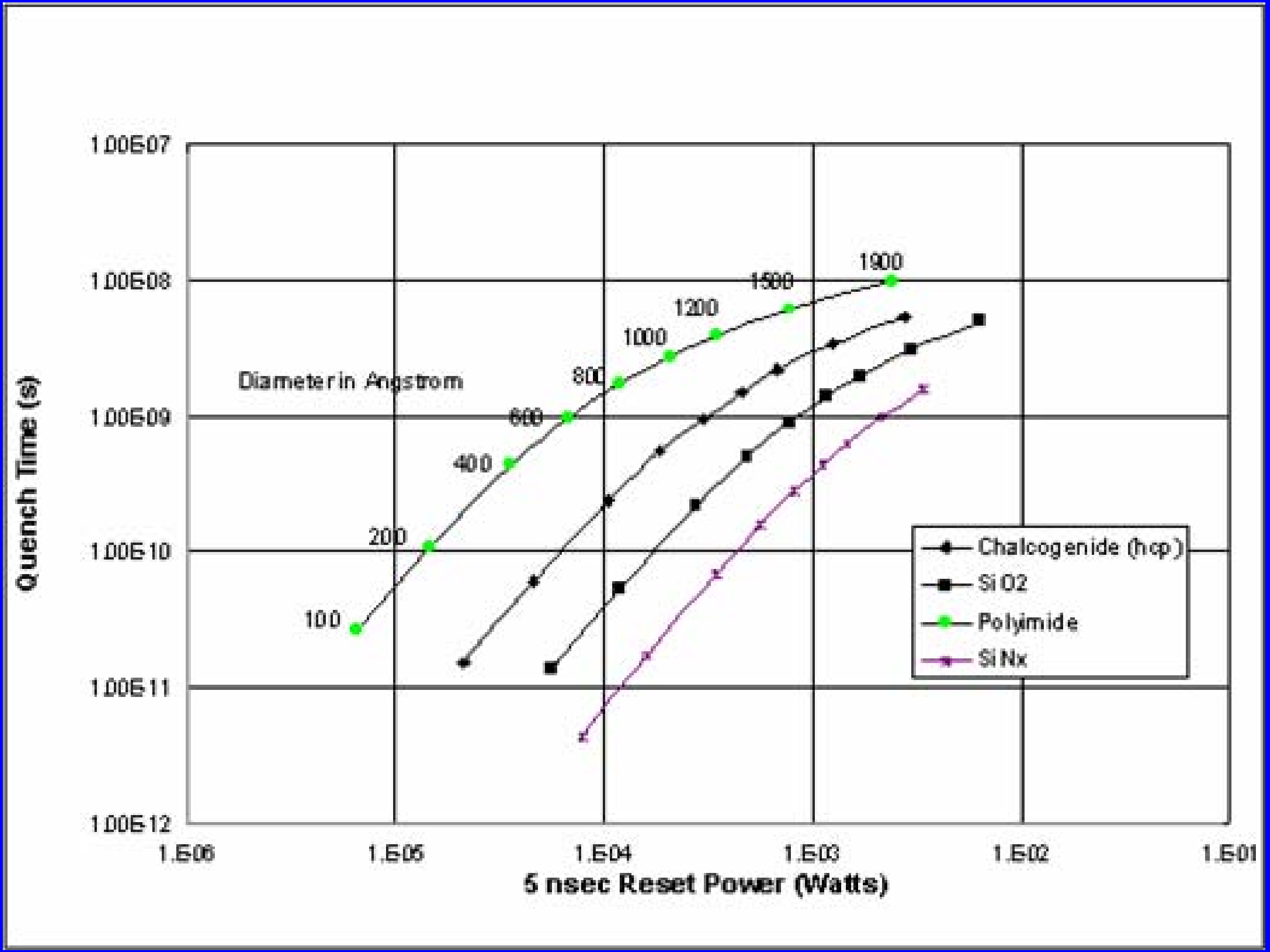


3D Temperature Profile of Heating

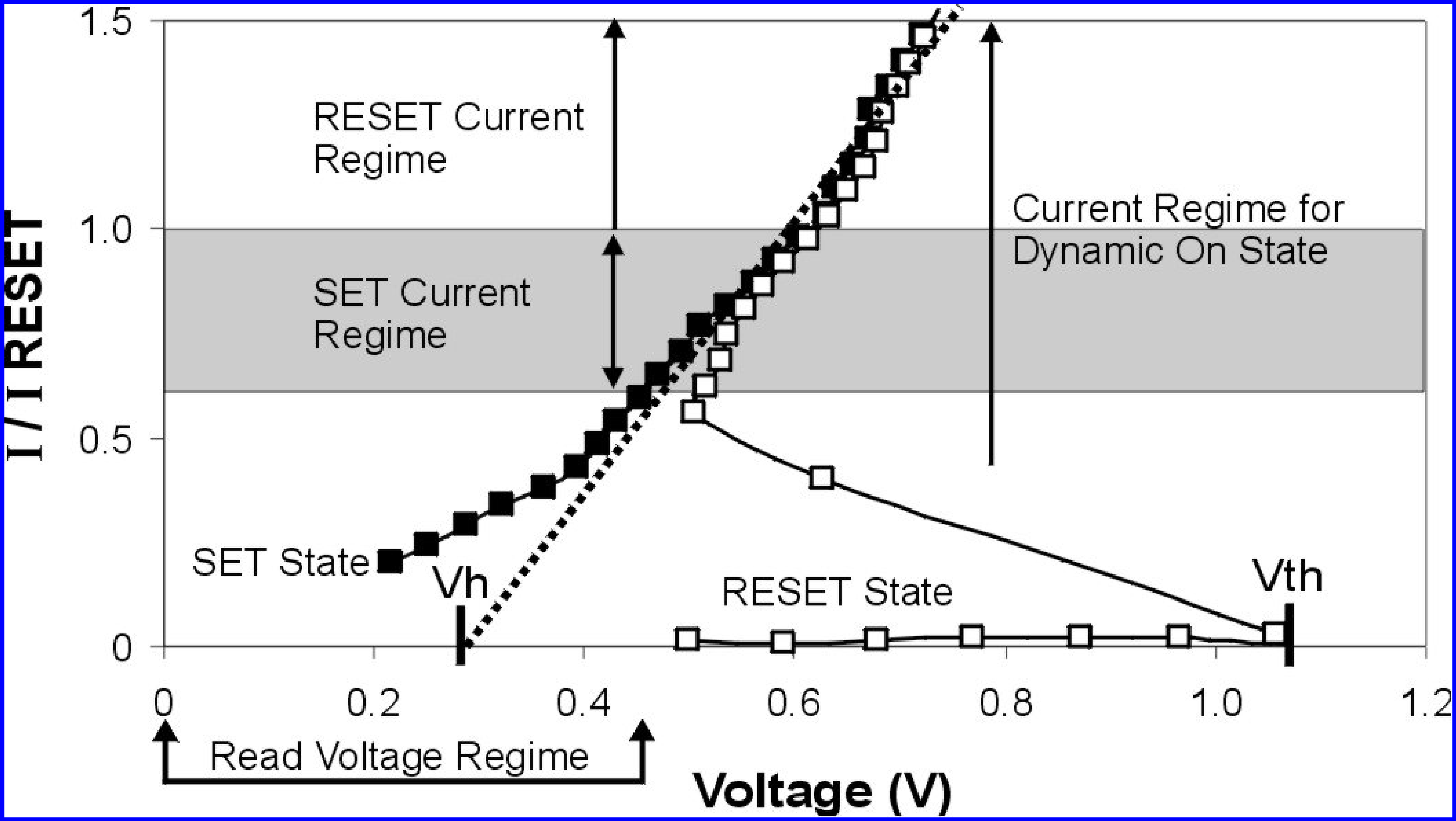


Heating of a 500A X 2000A device during a 20ns Reset Pulse

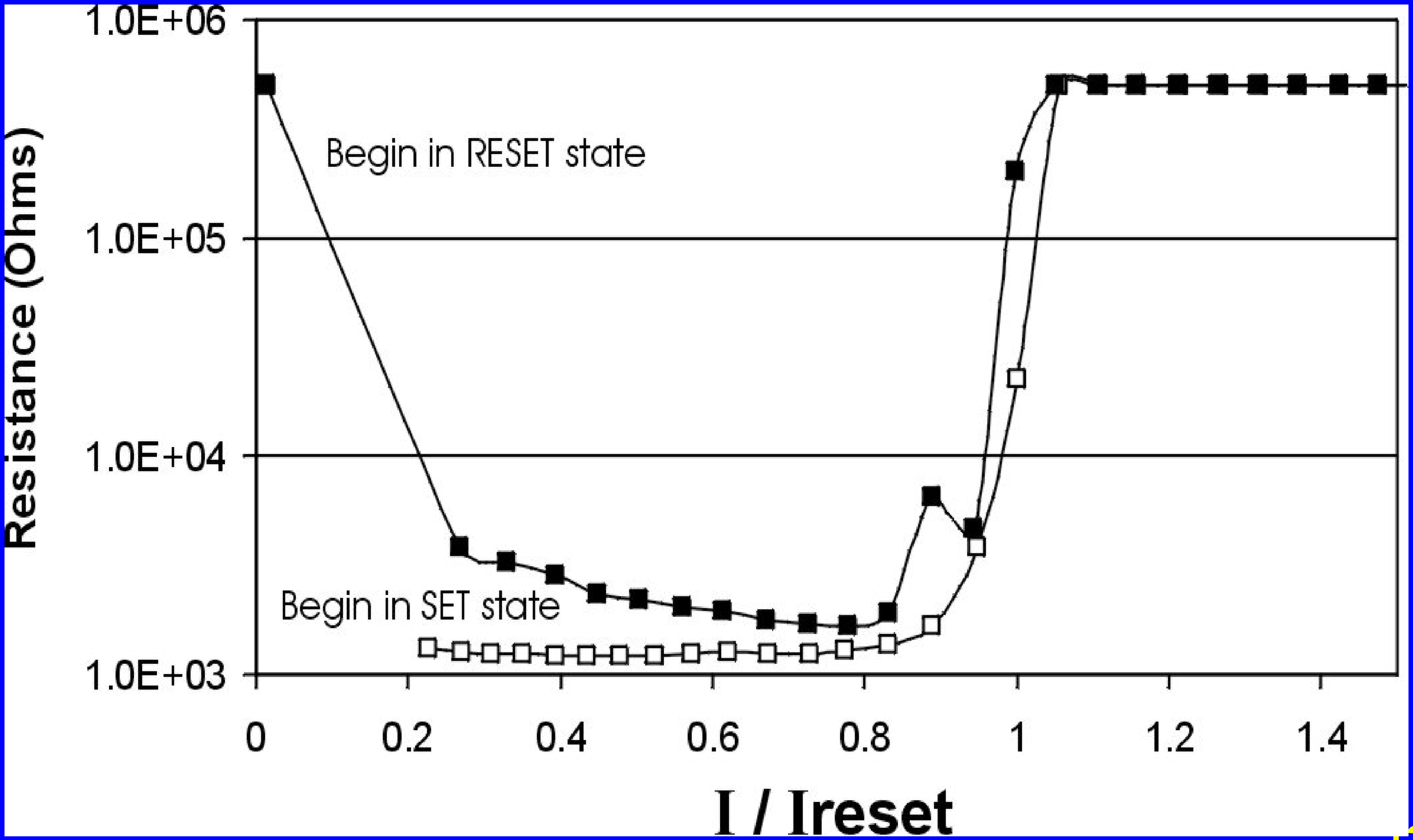
Simulated Impact of Thermal Environment on Programming Power



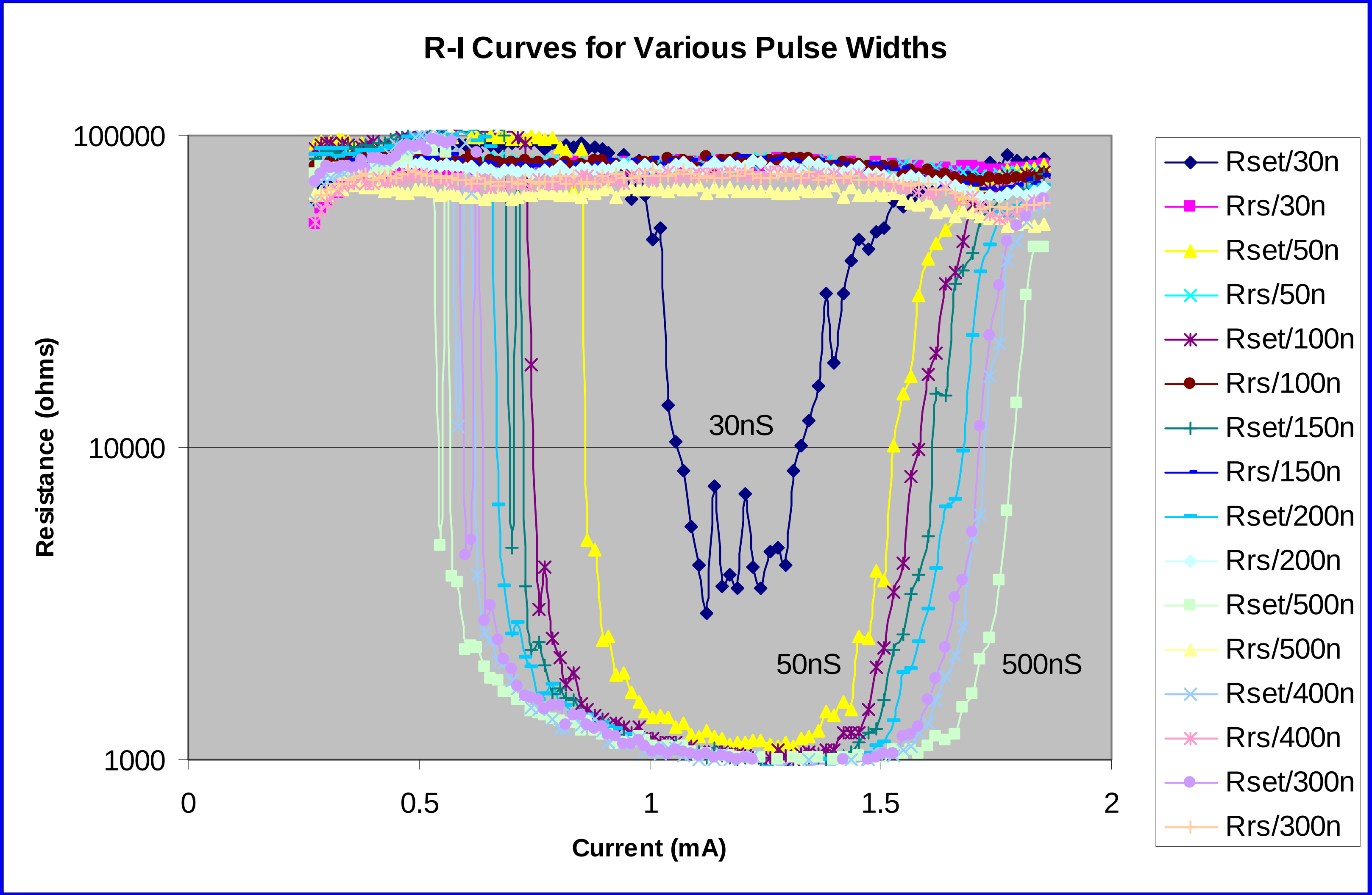
IV Curve of Chalcogenide Element



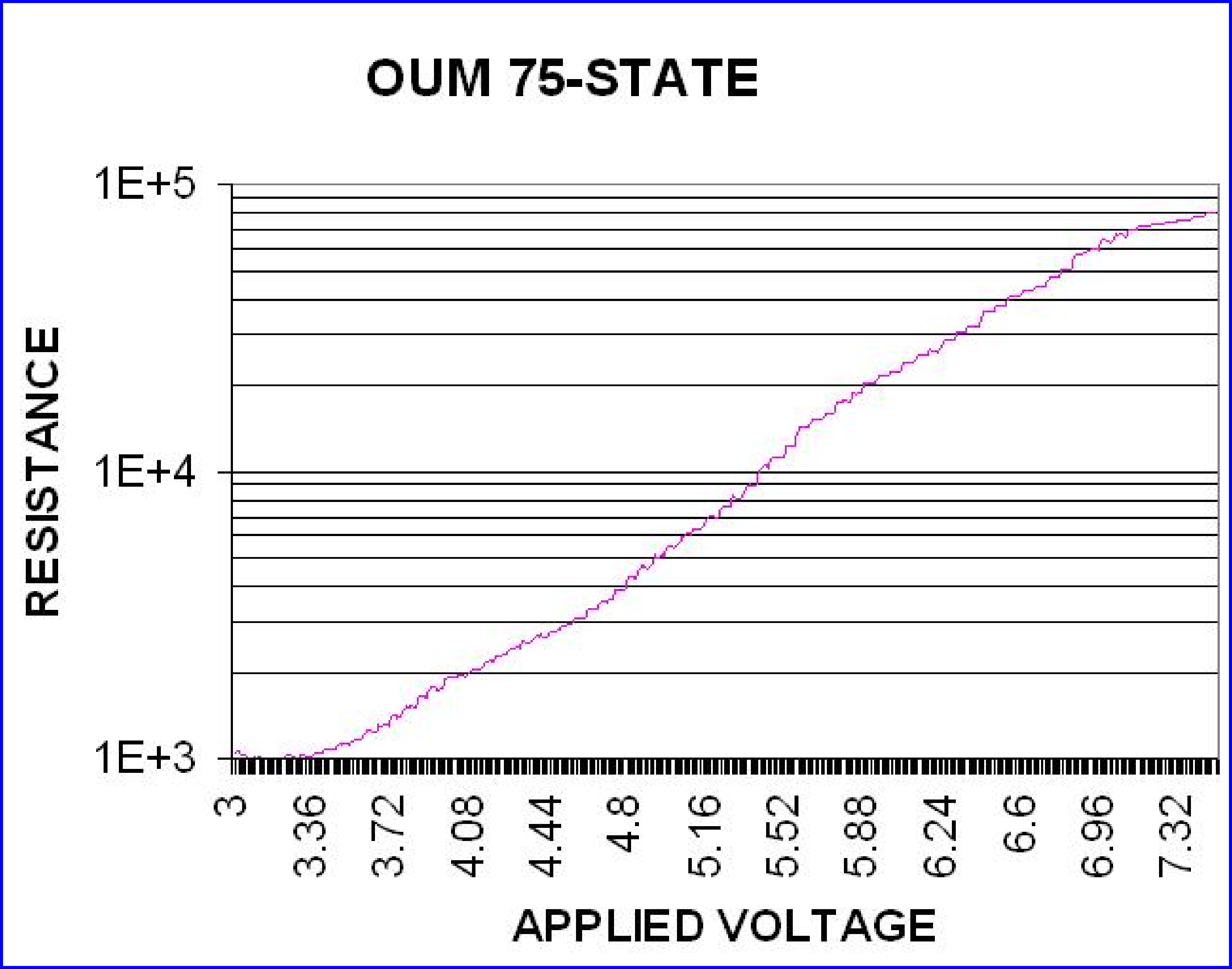
R_{set} and R_{reset} as Function of Cell Current



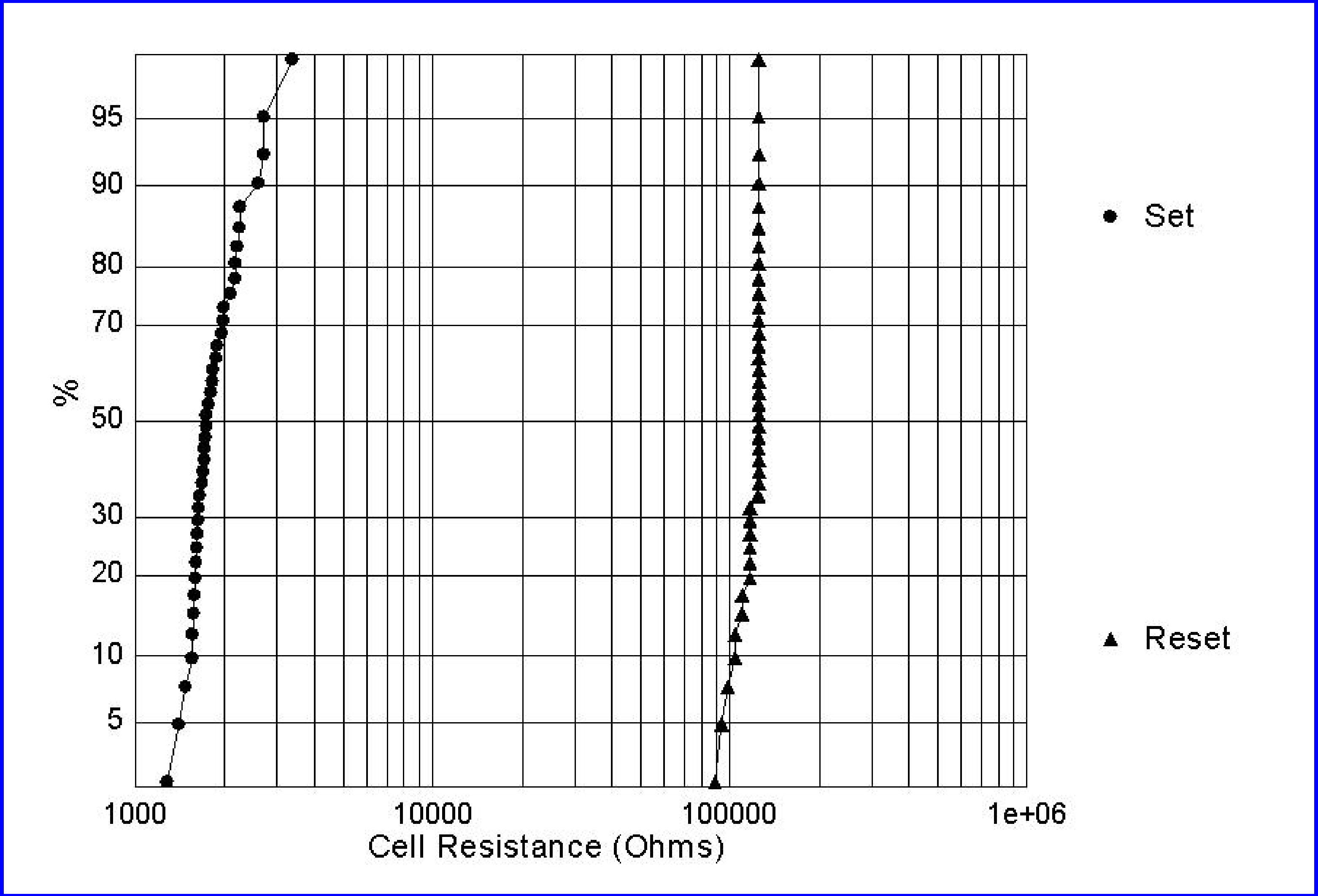
R-I Curve Dependence on Set Pulse Width



Analog Storage States



R_{set} and R_{reset} Distribution after 10^7 Cycles



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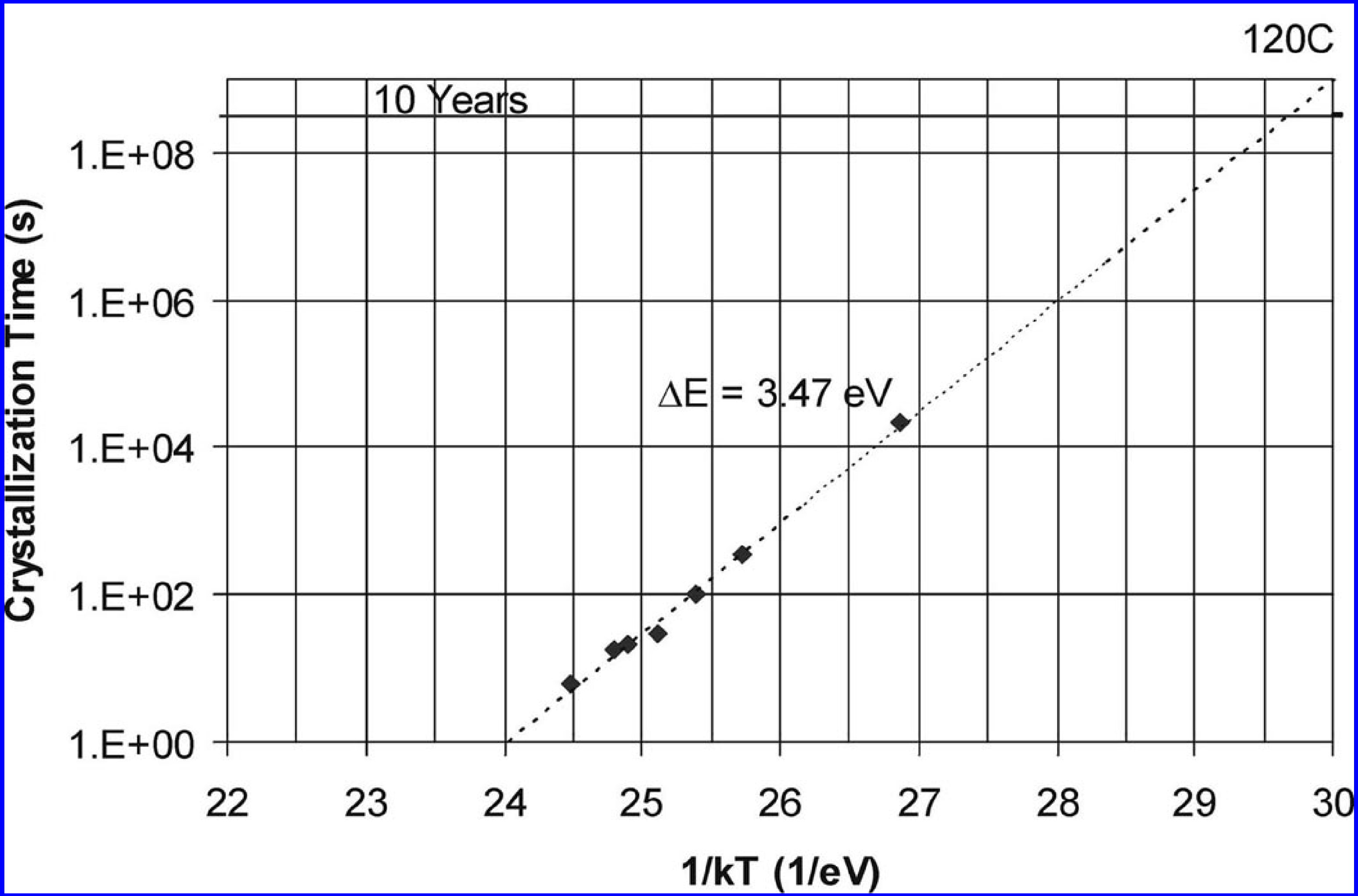
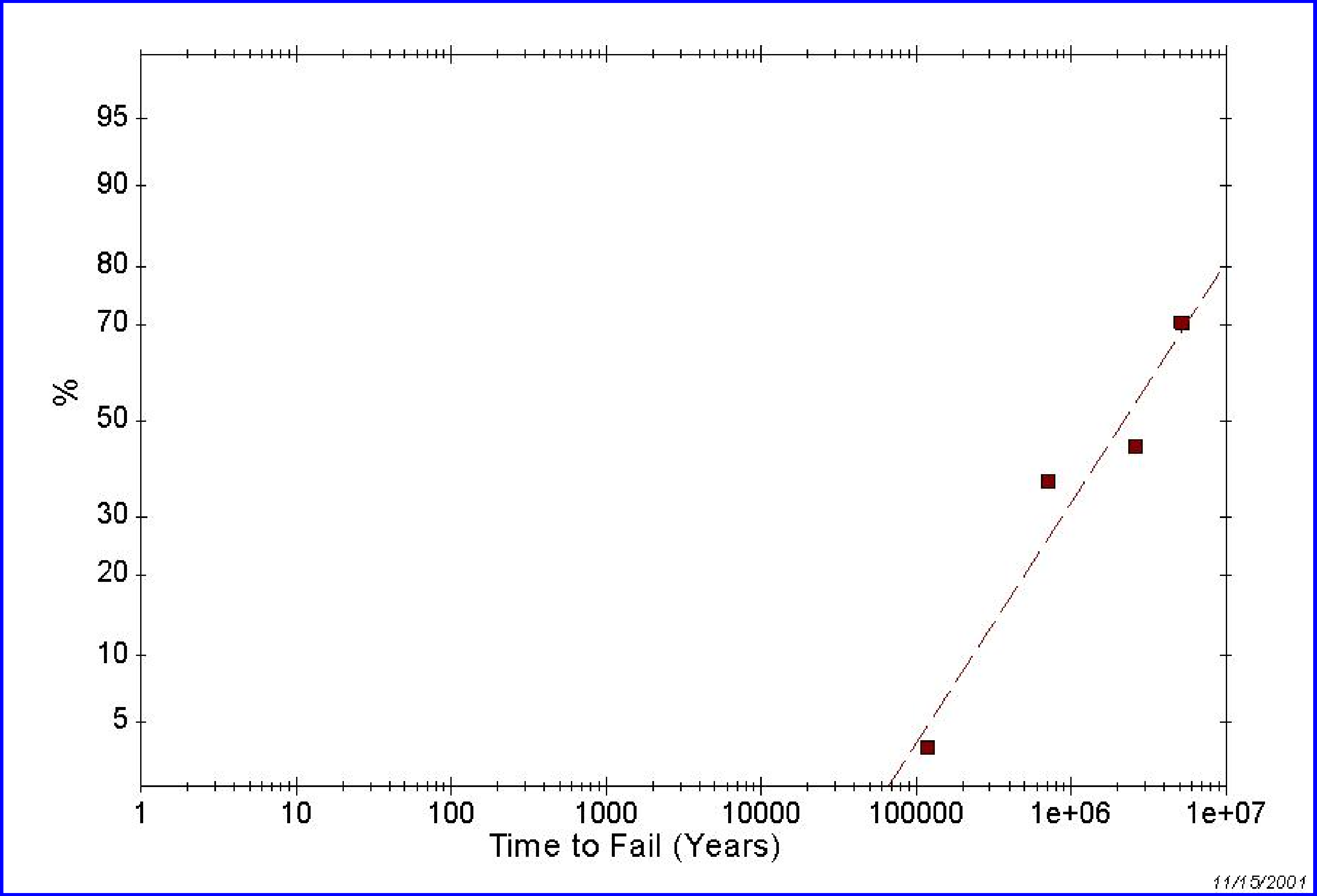
Reliability Considerations

- **Data retention: Retain data over time/temperature**
- **Endurance: Withstand set/reset cycles**
- **Disturb Immunity: Ability of cell to retain data in face of voltage transients**

Retention Characteristics

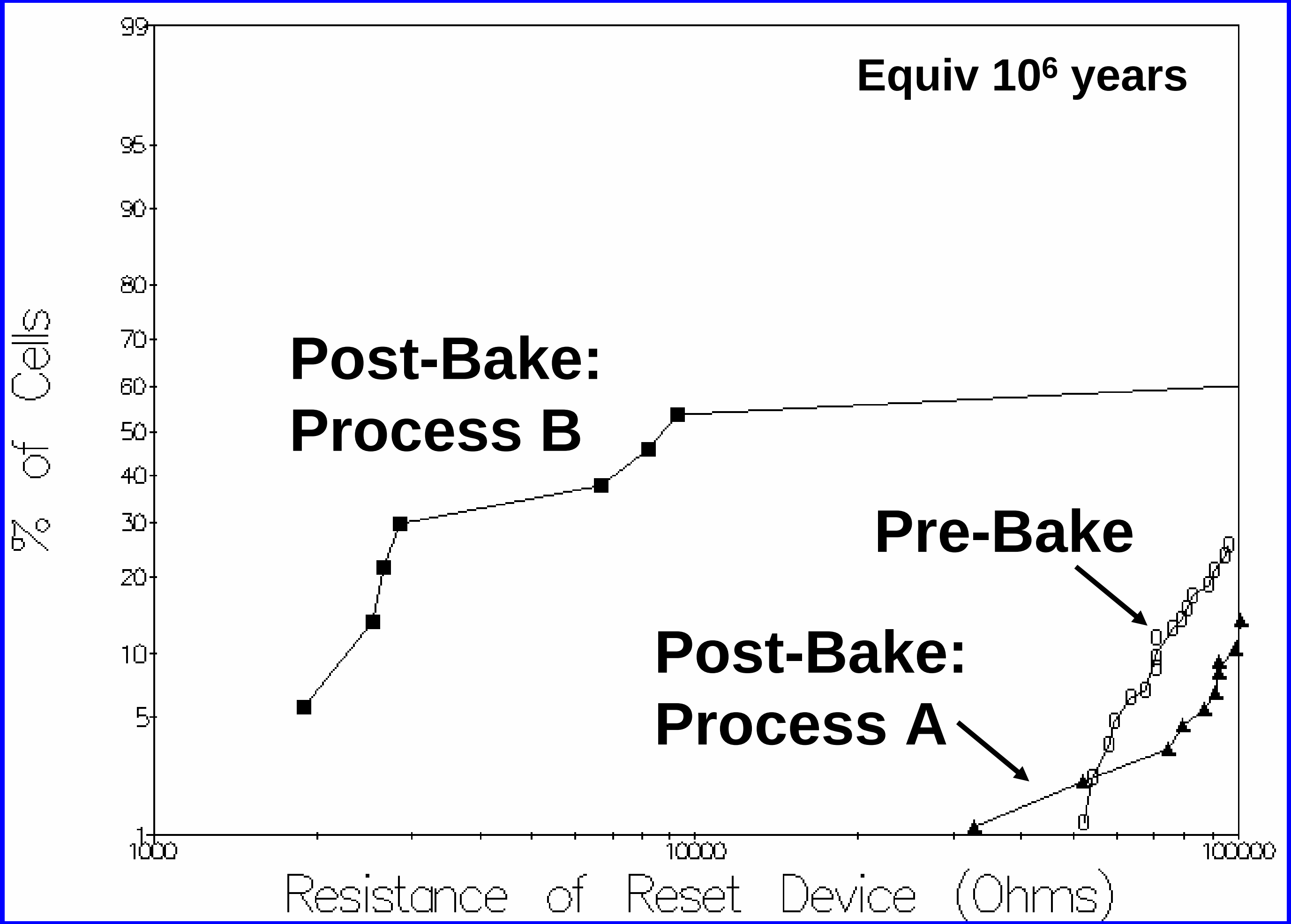


Retention at 70ºC after 10^7 Cycles



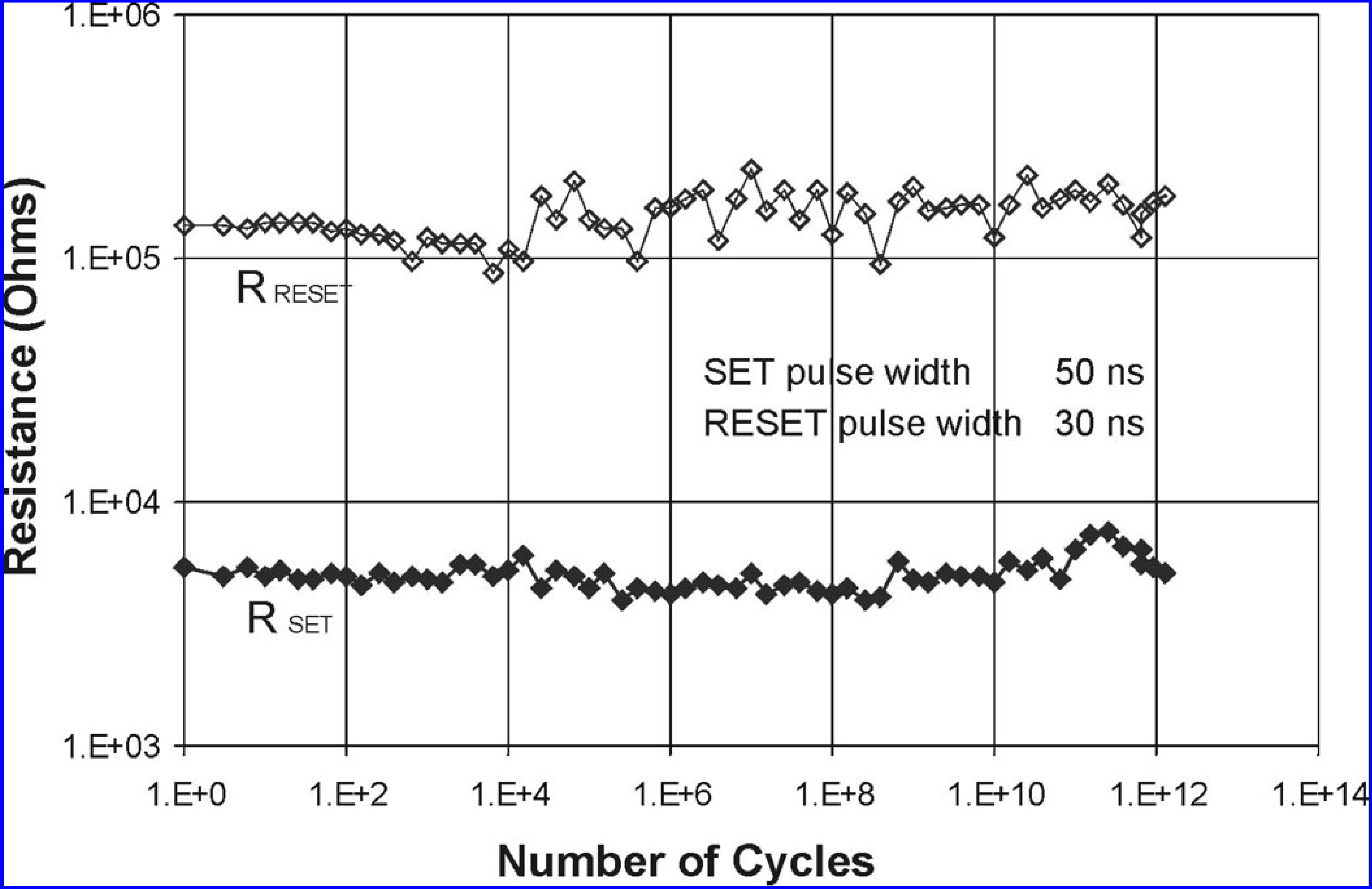
- **Capability: Many years data retention**

Retention for Non-Optimized Device



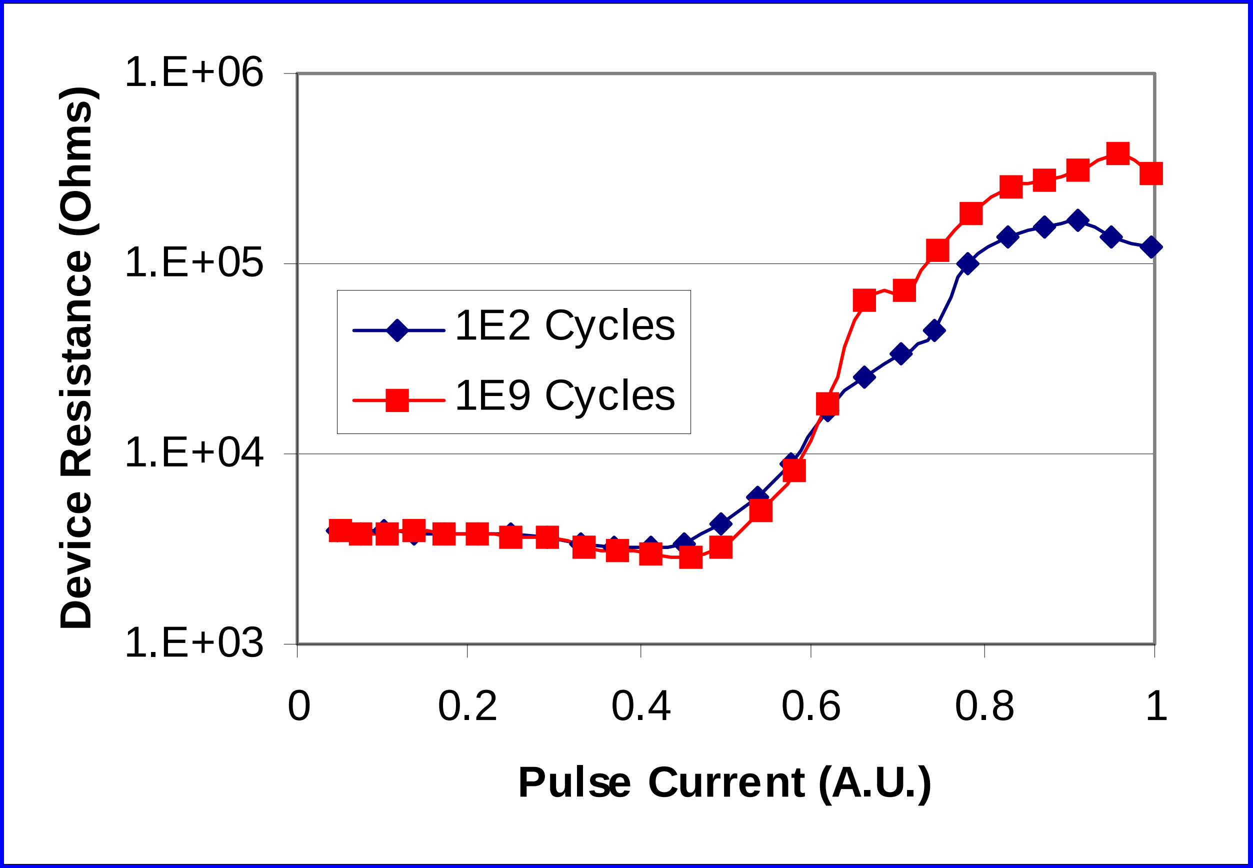
- Retention can fall short of capability with non-optimized processes

R_{set} and R_{reset} as Function of Cycles



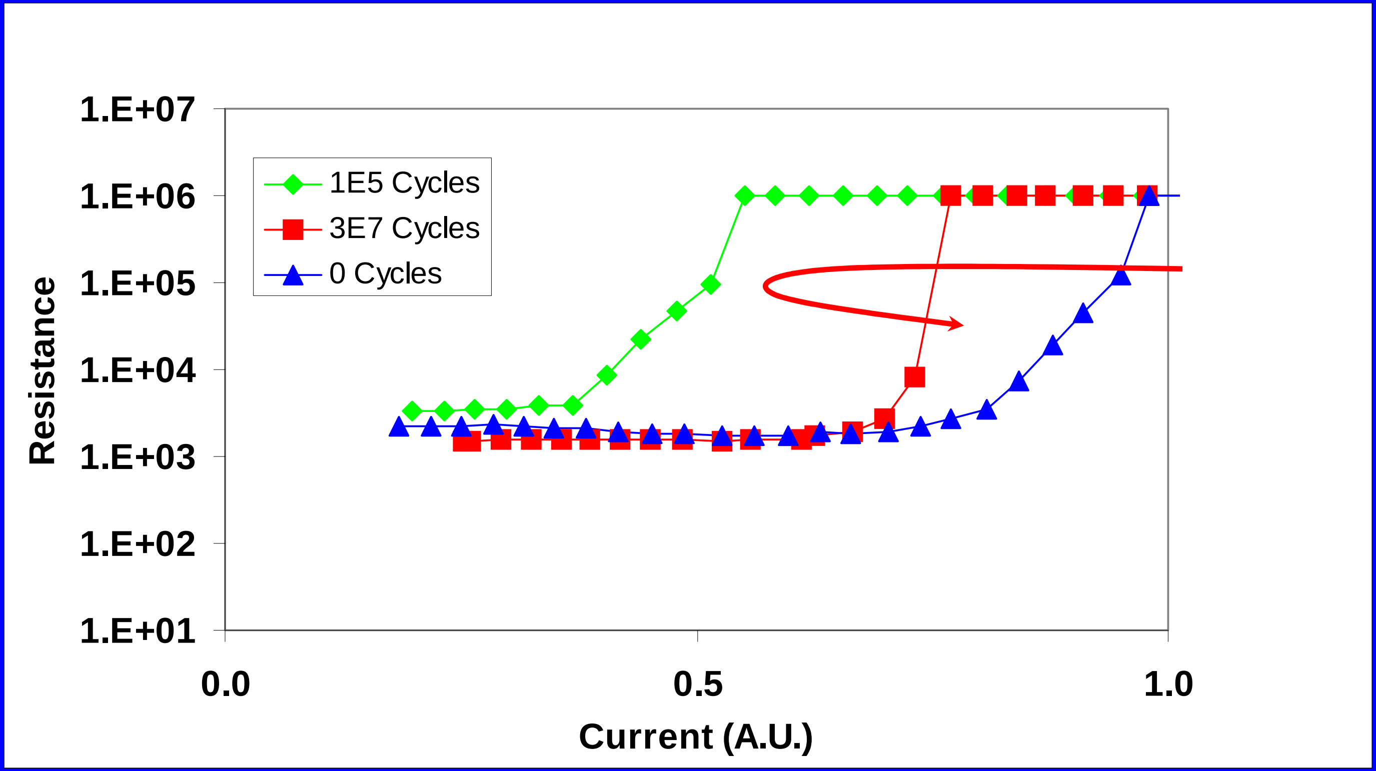
- **Capability: Stable window beyond 10^{12} cycles**

RI Shift after Cycling



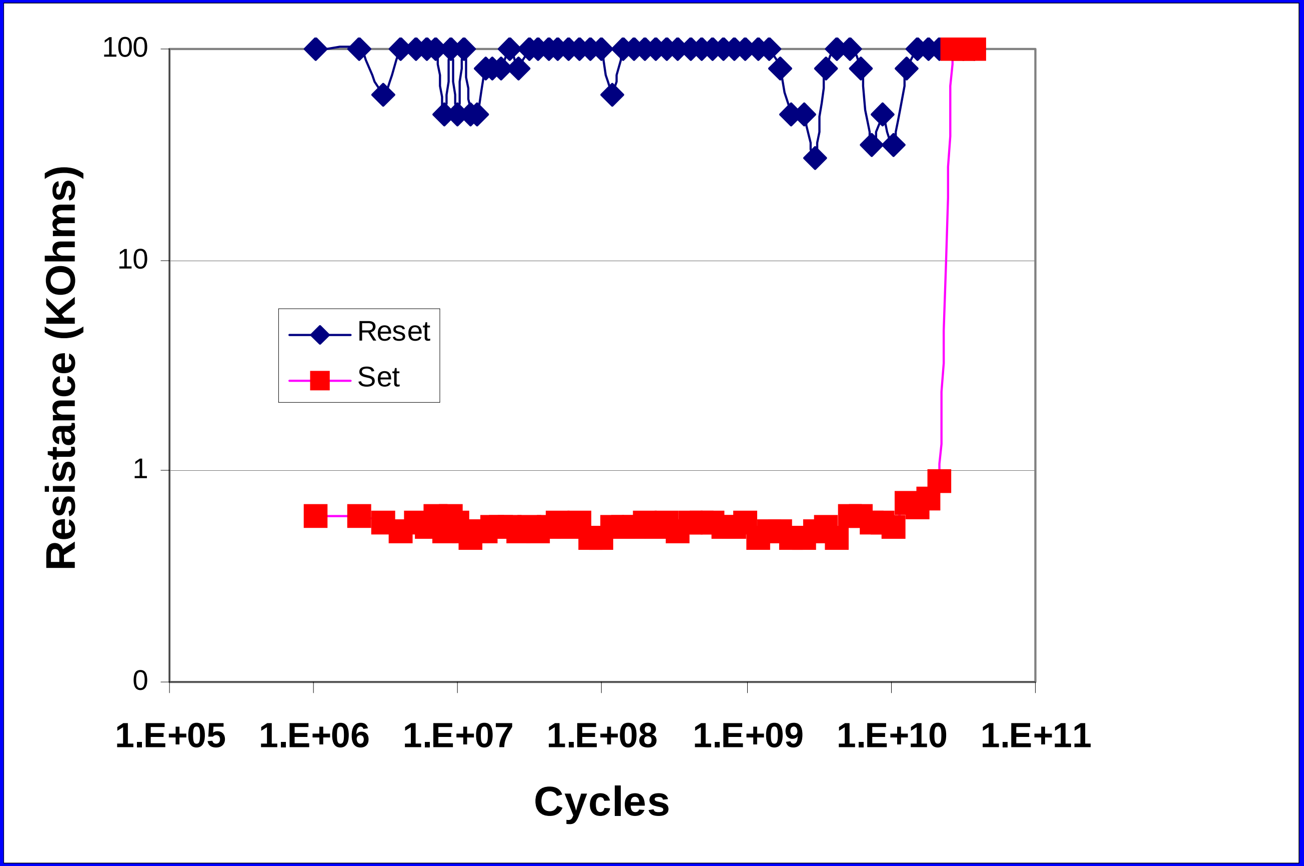
- **Capability: Stable programming characteristics**

Endurance: Reset Migration



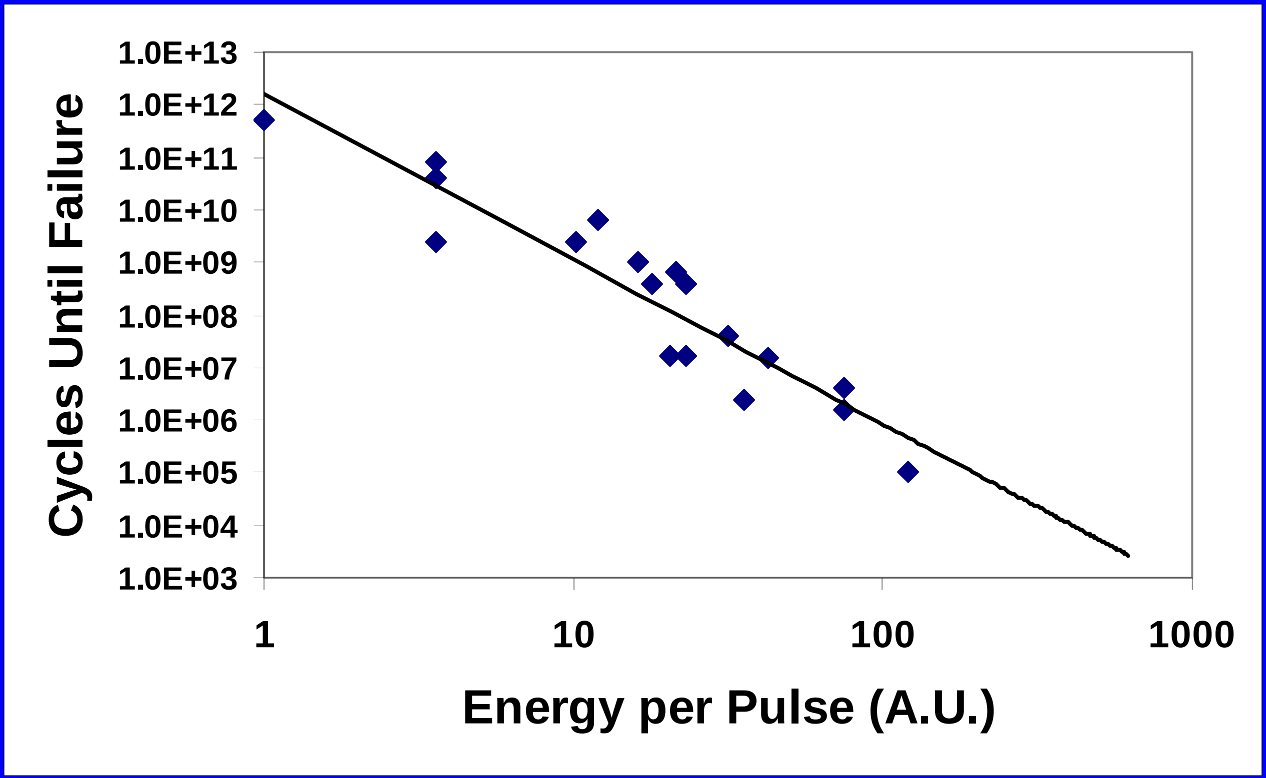
- **Walk-in of R-I characteristic with cycles**
- ***Some* migration always present in 1st two cycles (virgin chalcogenide has slightly different microstructure)**
- ***Severe* migration (above) occurs with non-optimized electrodes & interface quality**

Endurance: Stuck Reset



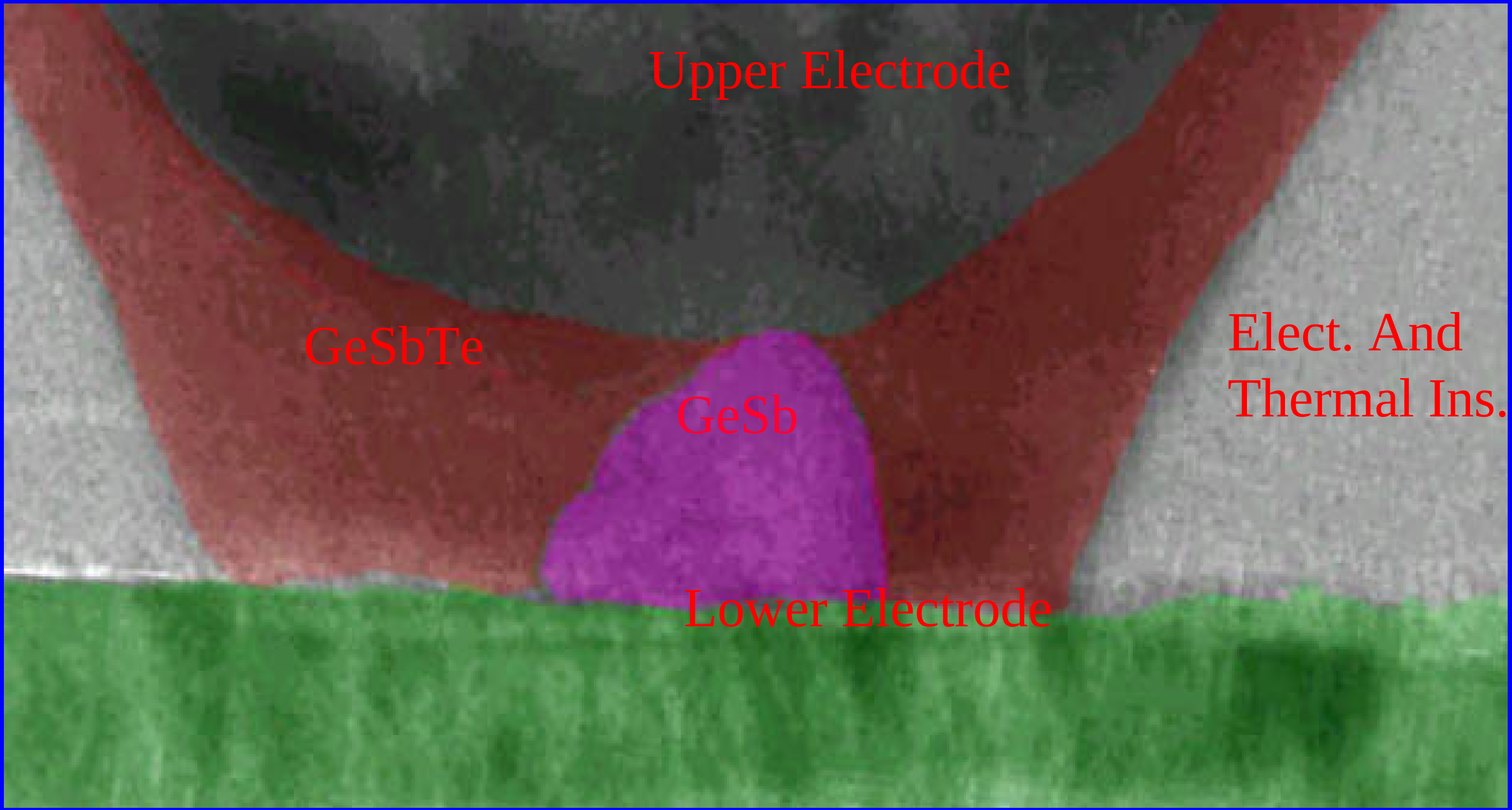
- **Often caused by physical separation of chalcogenide from electrode in non-optimized devices**
- **Example above is unpassivated cell**

Endurance: Stuck Set

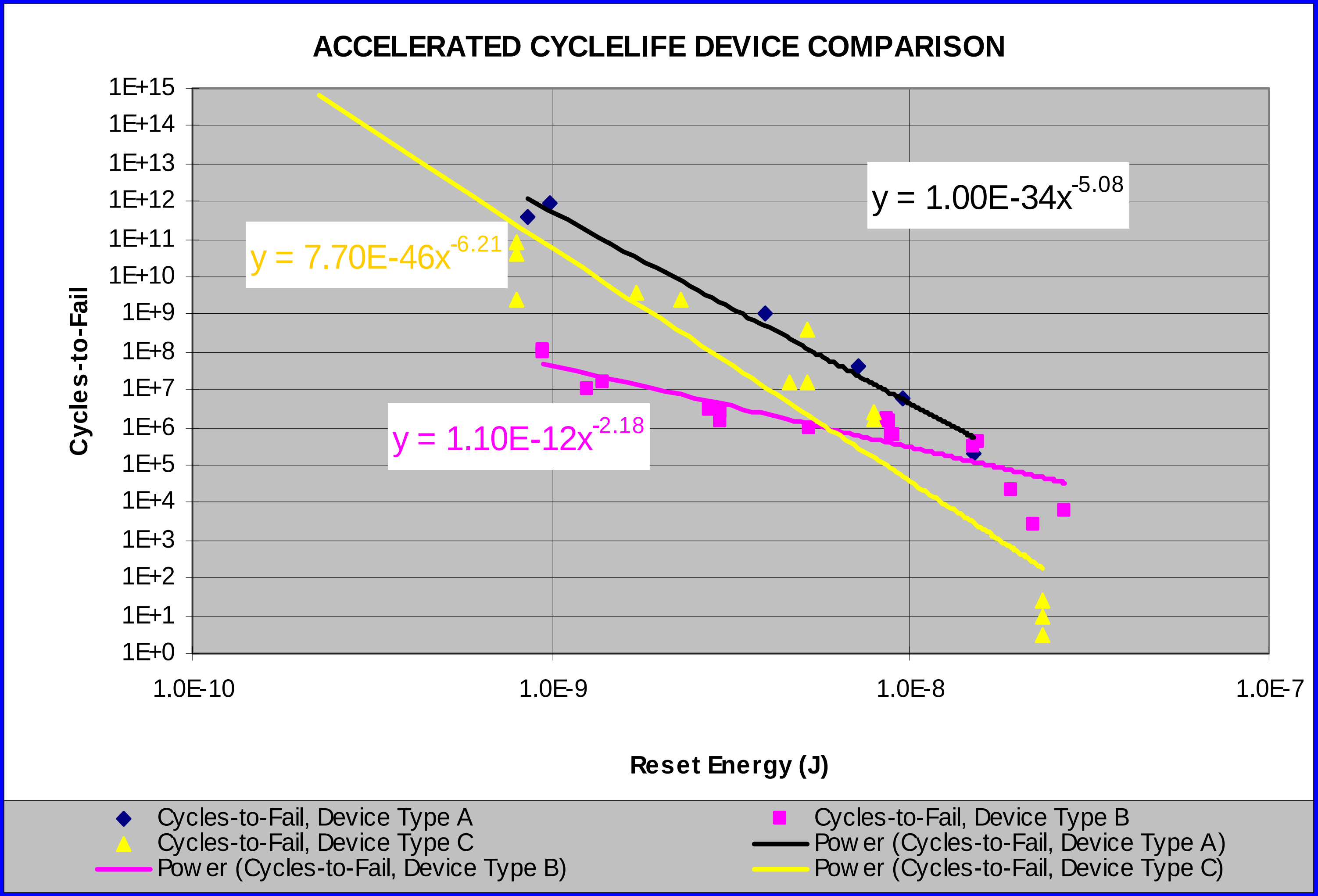


- Stuck set is more common failure mode (above)
- Endurance scales with energy per pulse
- Can occur when chalcogenide intermixes with adjacent materials
  - Strongly dependent on electrode & dielectric materials

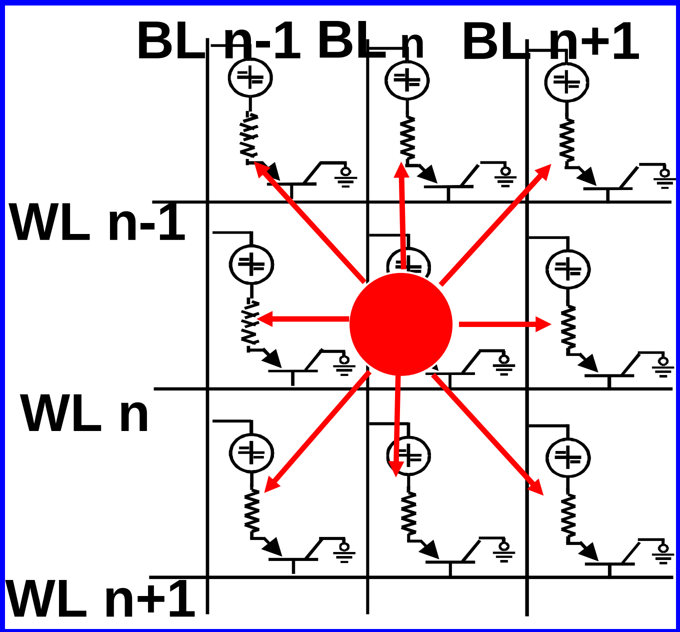
$5E^{10}$ Cycled to Failure with Over-current Reset

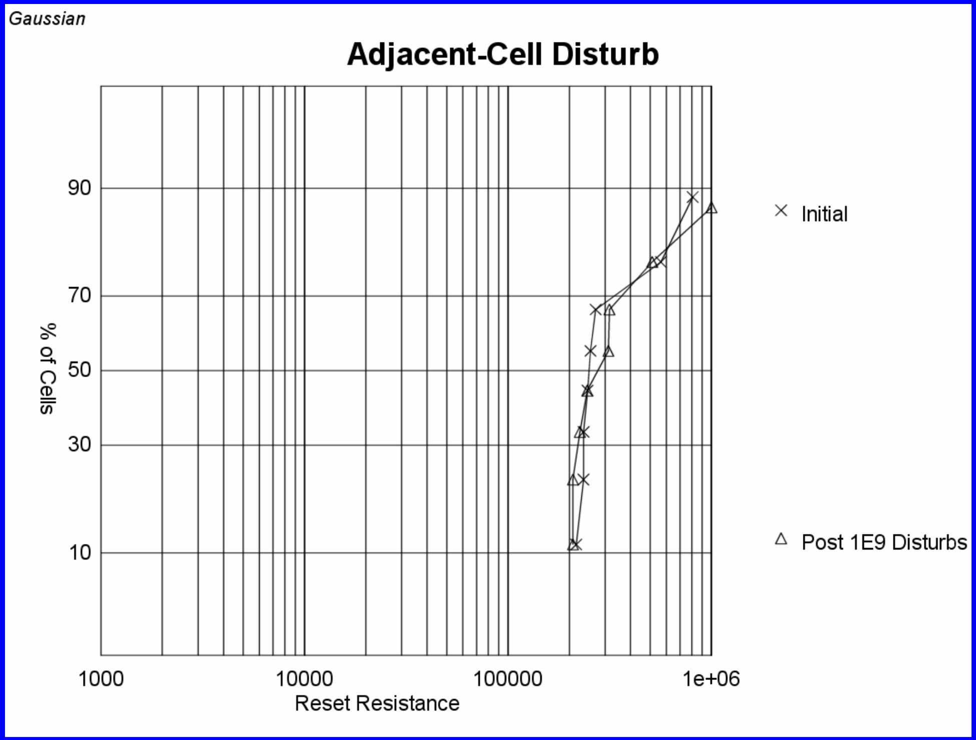


Accelerated Endurance Testing



Disturb Immunity





- Concern (left): Heat in cycled cell could spread to adjacent cell, converting reset to set
- Capability (right): No disturb over > 10^9 pulses

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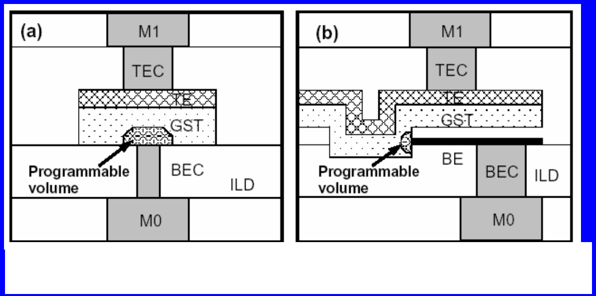
Edge Contact to Reduce Current



switching current

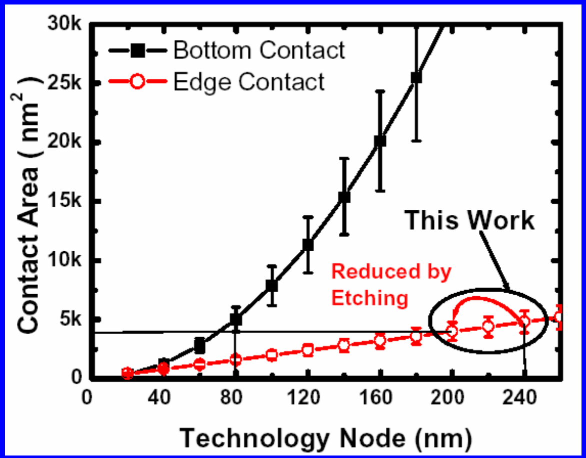


Figure 8: Edge contact current reduction

- **Key challenge in technology: lower Set and Reset current which is proportional to contact area**
- **Innovation: instead of litho defined, use thin film thickness => 75 nm node equivalent based on 240 nm node**

Material Engineering: Nitrogen Doping

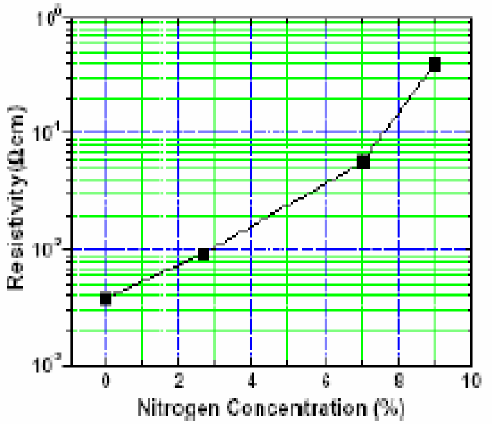


Fig.6 Resistivity of the GST films as a function of nitrogen concentration.

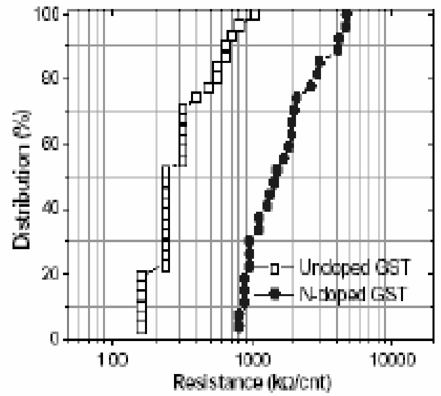


Fig.10 Distribution for the PRAM cell resistance for undoped and N-doped GST(N=7at%).

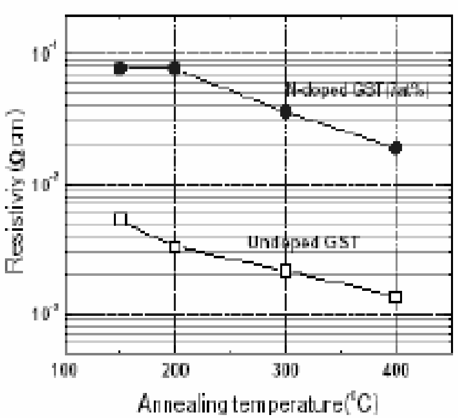


Fig.7 Resistivity of the (a) undoped GST and (b) N-doped GST(N=7at%) films as a function of anneal temperature.

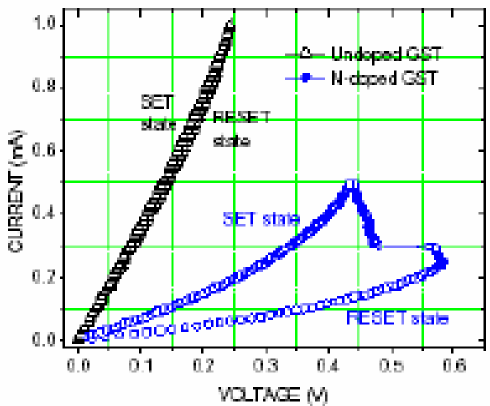


Fig.11 I-V characteristics of the PRAM cell after 2E7 cycles: (a) undoped GST and (b) N-doped GST(N=7at%).

- **Nitrogen doping increases GST resistance giving lower operating current**

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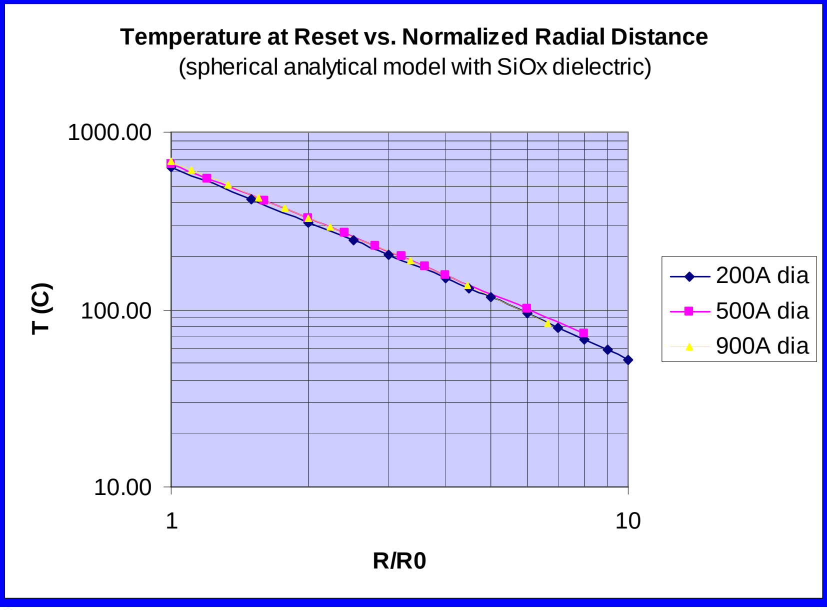
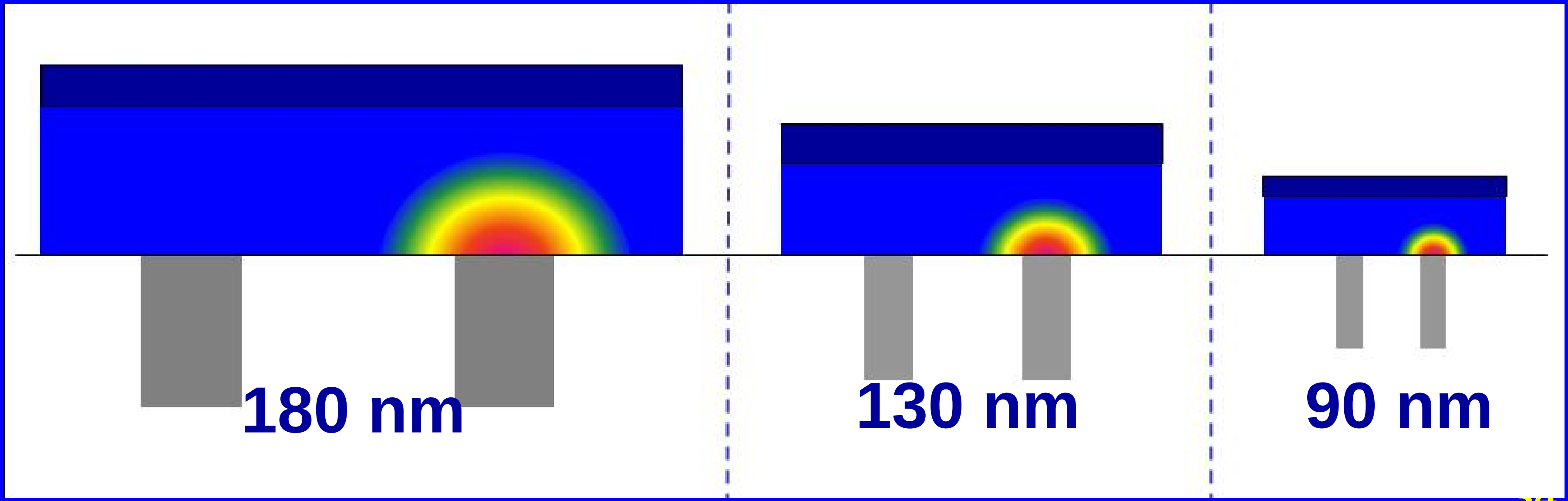
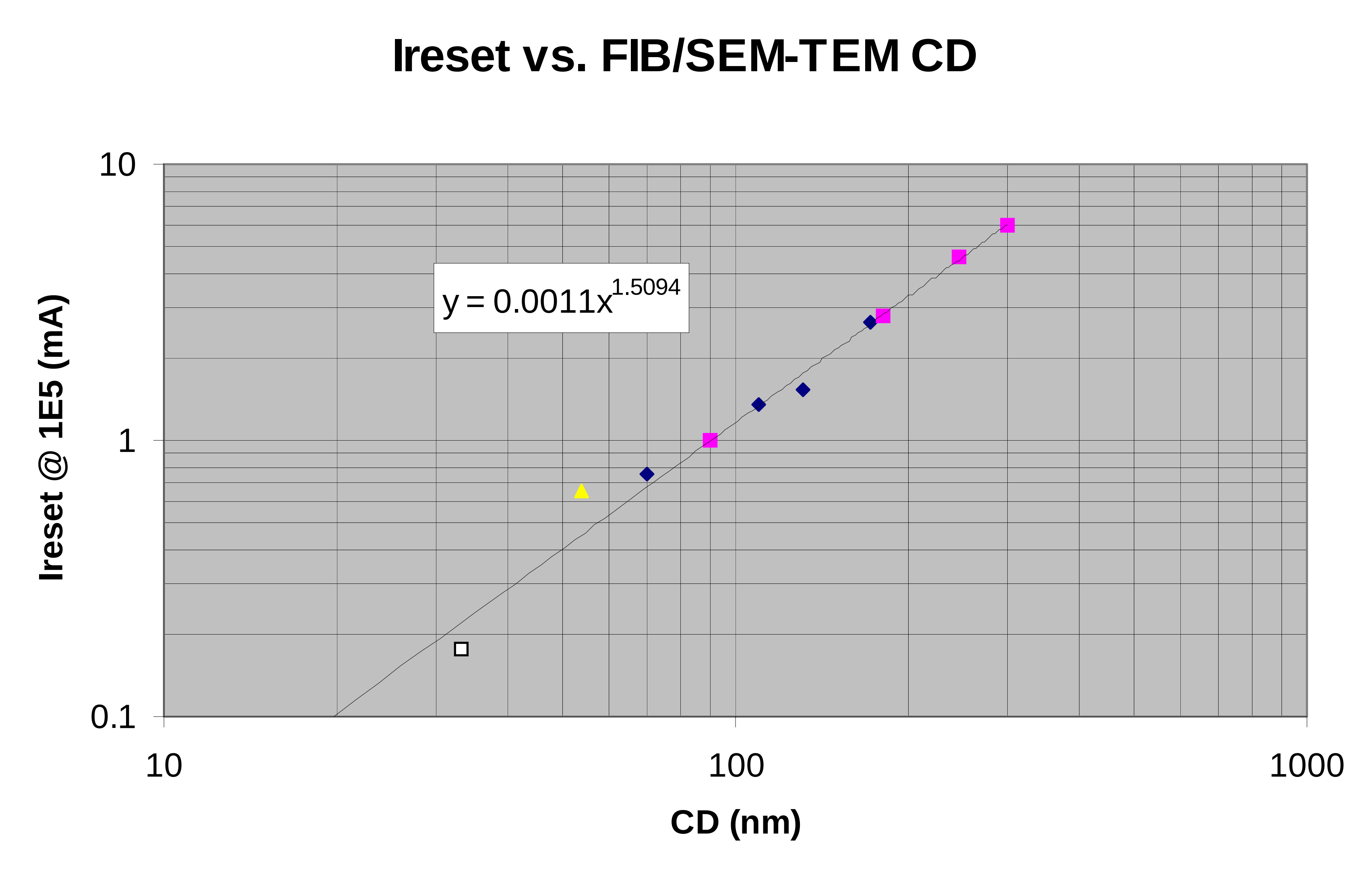
Disturb in Scaled Cell



- Contact area is scaled => Temp same with normalized radial distance



Ireset Scaling



Phased Change Memory Scaling
(constant Voltage)

		130 nm	90 nm	65 nm	40 nm	32 nm	22 nm	Scaling Percent	Comment
DRAM 1/2 Pitch	nm	130	90	65	45	32	22	-30%	Moore's Law
Electrode Contact Dimensio	nm	47	33	23	16	11	8	-30%	Sublitho Dimension Scales with Moore's Law
Ireset	μA	500	294	171	99	57	35	-41%	From actual data and extrapolated
Chal thickness	nm	60	50	40	30	30	30	-13%	Scale for AR, min 30nm for Spreading R
Rset Chal	KΩ	1.6	2.5	3.8	5.5	9.6	12.2	50%	Spreading resistance model
Rset Electrode Heater	KΩ	0.8	1.4	2.3	4.0	7.1	11.4	70%	0.4V heater voltage
Rset Total	KΩ	2.4	3.9	6.1	9.5	16.7	23.6	58%	Chal + Heater
Diode area	nm^2	18590	8910	4648	2228	1091	535	-51%	Cell diode area = 1.1 square features
Deep trench depth	nm	440	396	356	321	289	260	-10%	Process Assumption
Buried WL Depth	nm	390	351	316	284	256	230	-10%	Process Assumption
Shallow trench Depth	nm	200	180	162	146	131	118	-10%	Process Assumption
P+ Junction Depth	nm	120	108	97	87	79	71	-10%	Process Assumption
Vertical Diode Depth	nm	270	243	219	197	177	159	-10%	Buired WL-P+ junction
Wordline depth under trench	nm	190	171	154	139	125	112	-10%	Buried WL-Shallow trench
Diode J vertical	A/cm^2	2.69E+00	3.30E+00	3.68E+00	4.46E+00	5.19E+00	6.57E+00	20%	Increases with smaller diode area
Diode vertical IR drop	V	0.070	0.077	0.078	0.085	0.089	0.101	8%	Vertical scaling offsets current increase
Buired WL J lateral	A/cm^2	2.02E+04	1.91E+04	1.71E+04	1.59E+04	1.44E+04	1.42E+04	-7%	Decreases with I reset
Buried WL lateral IR drop	V	0.20	0.12	0.07	0.04	0.02	0.01	-41%	Decreases with smaller Cell
Dioide Forward Voltage Drop	V	1.37	1.30	1.25	1.22	1.21	1.21	-2%	Small change in Voltage drop

Scaling Summary

- Assume constant operating voltage
- Contact area scales with technology node
- Diode junction depth scales 10% per generation
- Conclusion: resistance goes up >50% per node; but within limit of advanced circuit capability
- No other physical scaling limit

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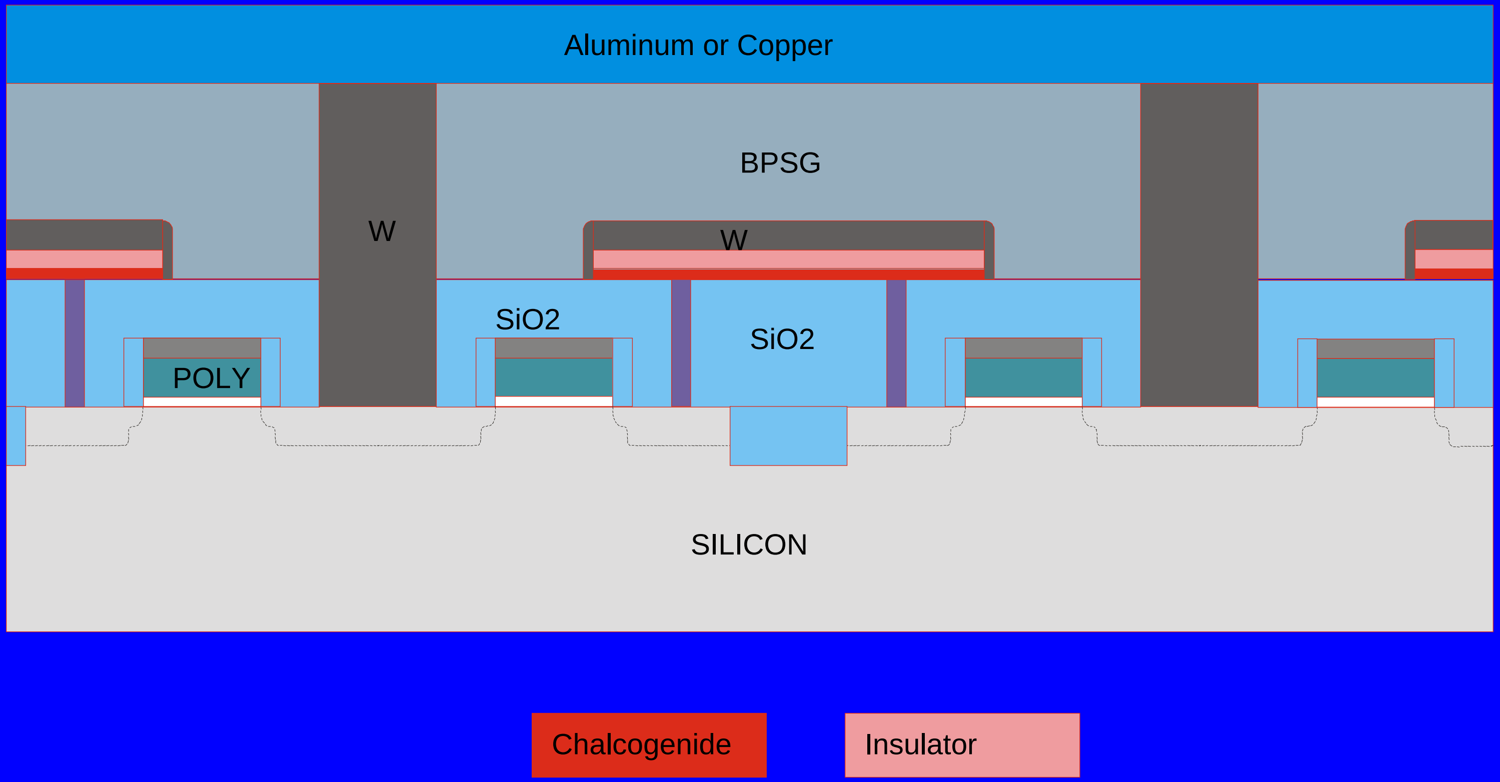
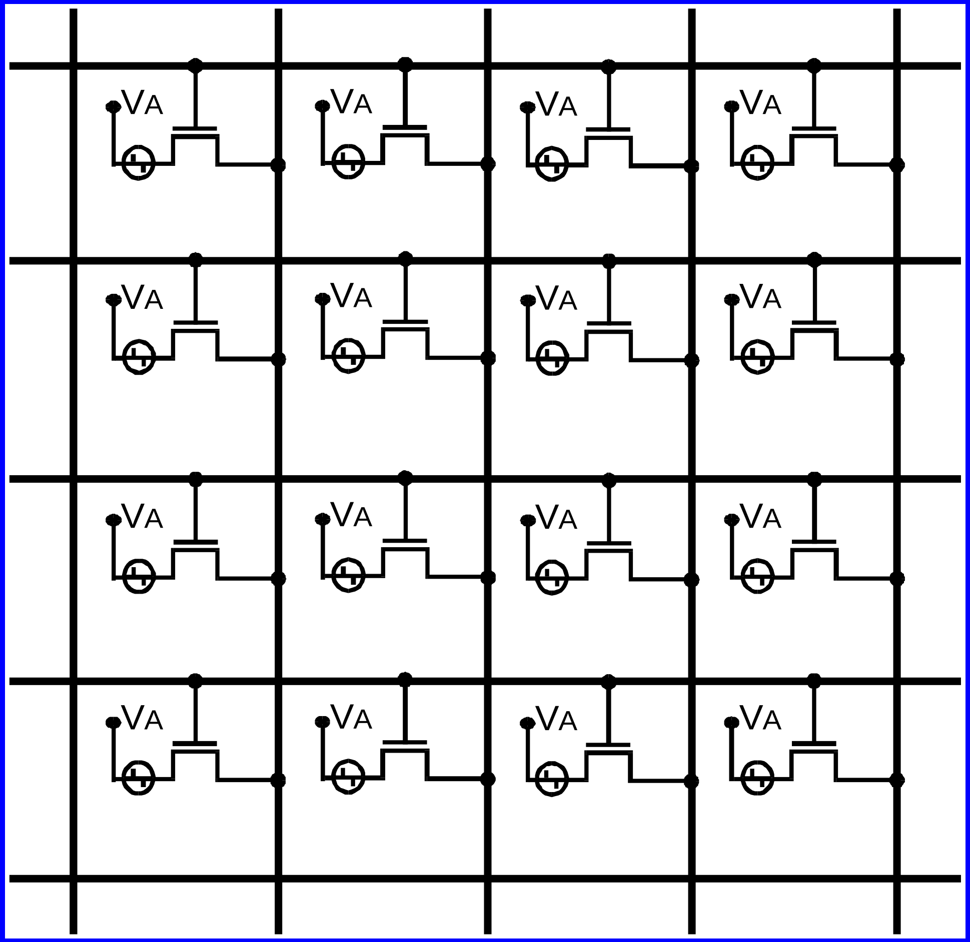
Transistor Selection



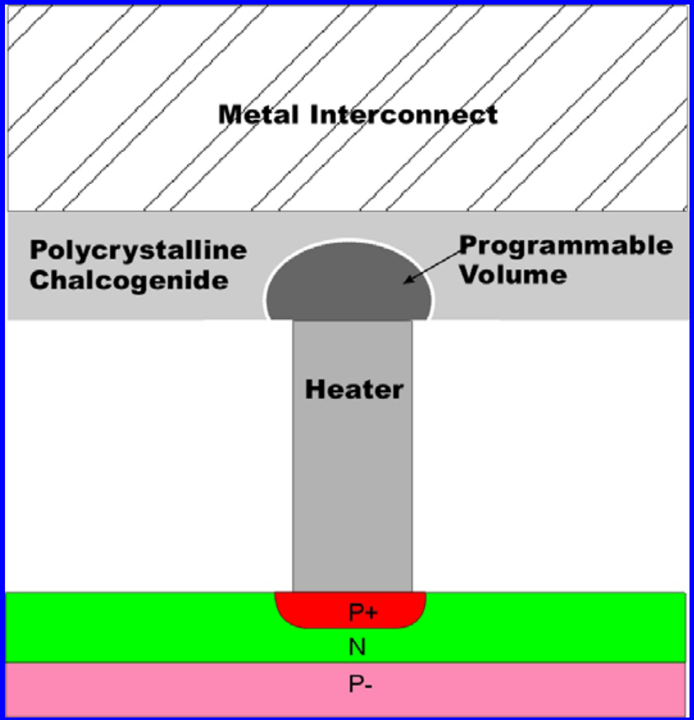
- Chalcogenide memory is a variable resistor requiring a selection device in memory array
- A NMOS transistor can be used: best array isolation

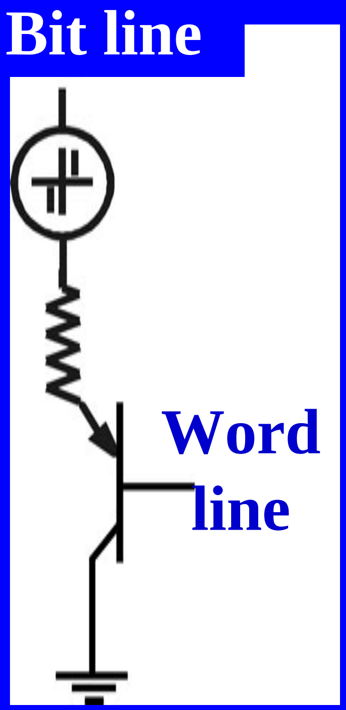
Array with TR selection



- Conventional array architecture similar to DRAM
- Clean cell to cell isolation with high on/off ratio
- Select TR must support full program current, not a minimum dimension device

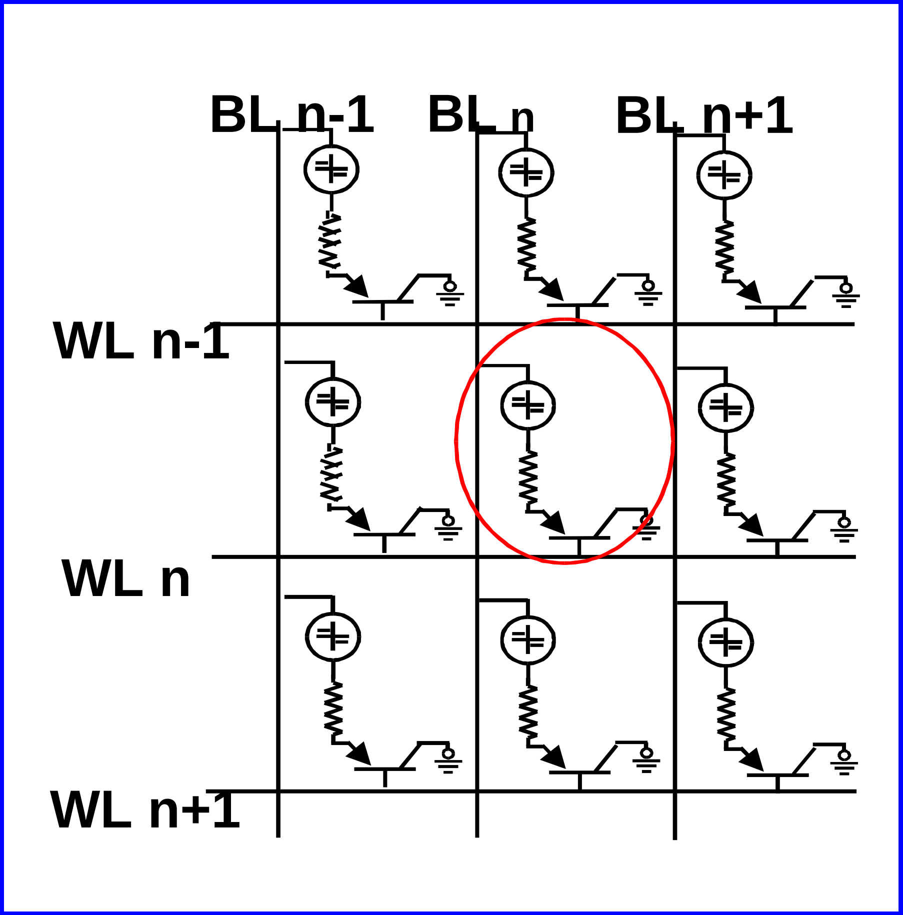
Junction Diode selection





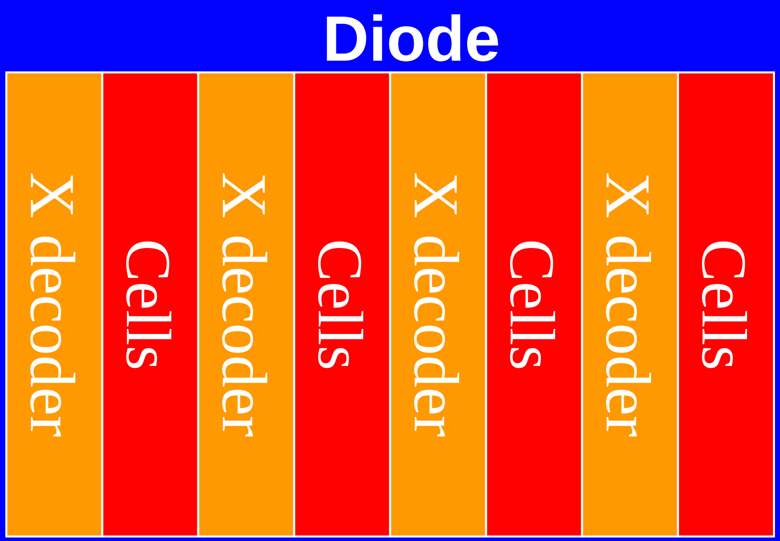
- To get to the smallest area, diode selector can be used: diode can carry much more current
- A parasitic transistor is formed with standard CMOS process, finite amount of current optimization

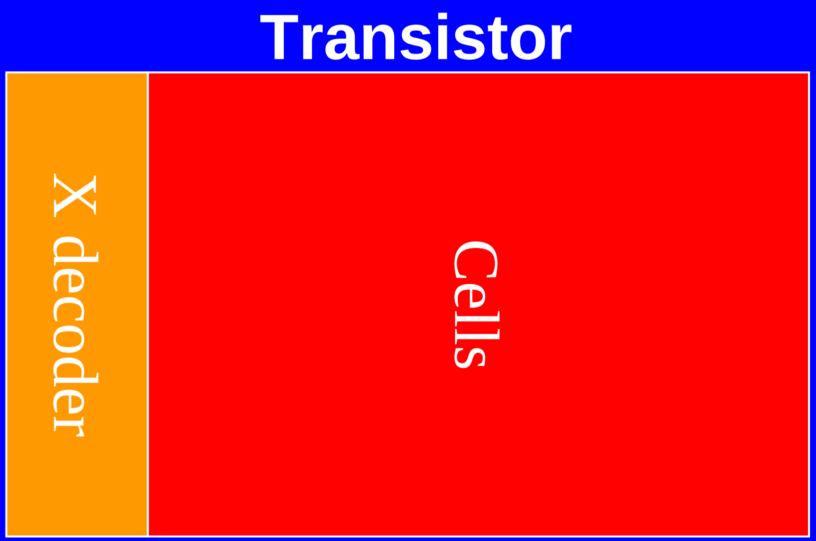
Array with Junction Diode Selection



- Smallest cell layout
- Both bitlines and wordlines have to carry relatively high current => have to subdivide columns to handle the current
- Parasitic resistance in full signal path important, both series and leakage currents contribute to error

Array Comparison (not to scale)





- Diode selector has smaller cell area
- High current required for cell through X decoder -> smaller column width to carry current

- Transistor selector has larger cell size depending on technology generation
- Smaller X decoder and wider column

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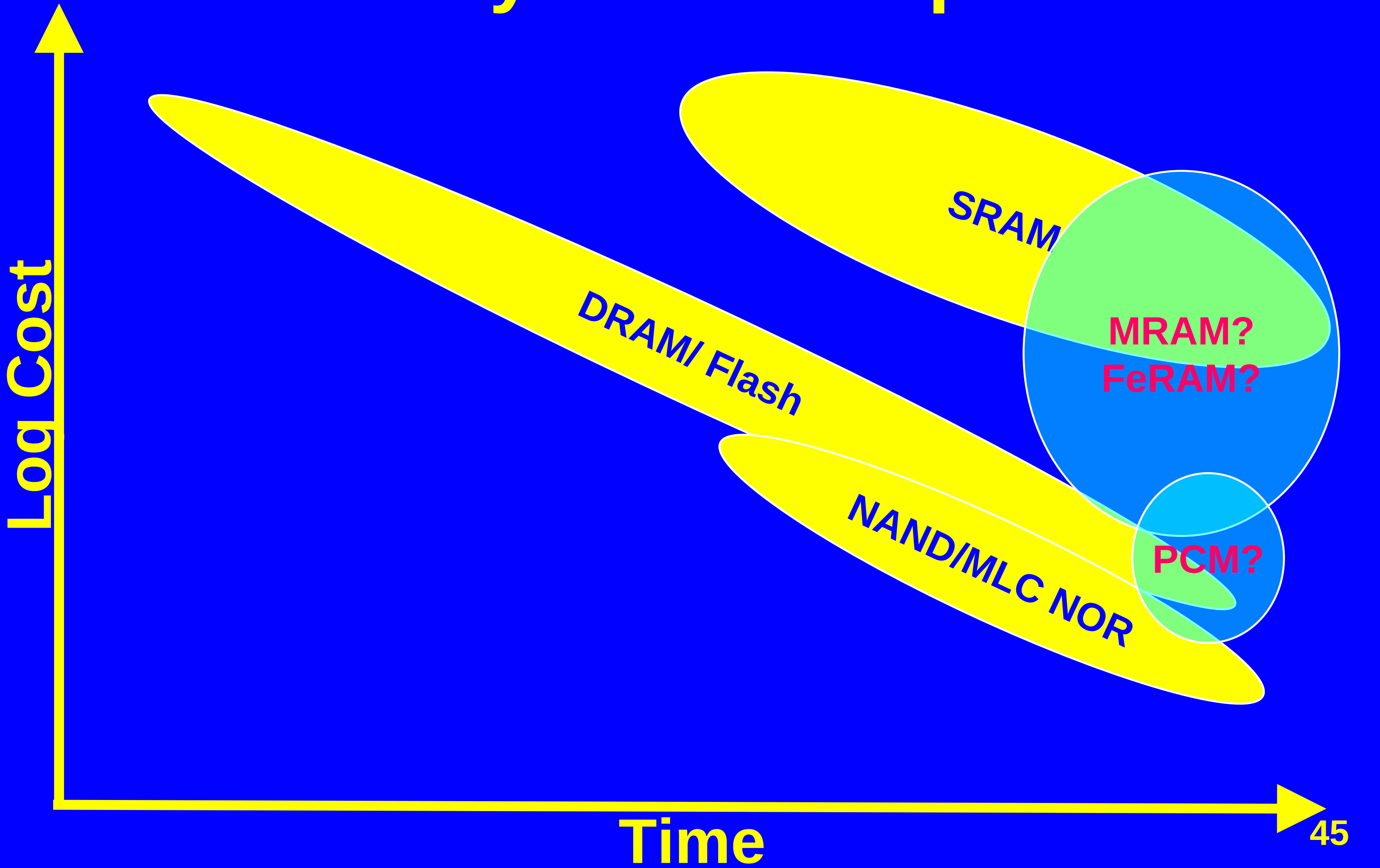
Memory Cost Comparison



Summary

- Phase change memory based on chalcogenide memory has been demonstrated
- With no known physical scaling limit, it has the potential to continue Moore’s law scaling beyond transistor memory scaling
- In the near term, projected cost is high compared to NOR/NAND flash: challenge is to how to lower cost faster